IN THE CLAIMS

Please cancel claim 4.

Please amend claim 5 as follows.

For the convenience of the Examiner, all pending claims are reproduced below including claims that are unchanged by this Amendment.

SUB C17

1. (unchanged) A method for sizing a database management system, the method comprising the steps of:

providing one or more percent hardware utilization limits;

obtaining throughput workload requirements; and

calculating the hardware resources needed to satisfy the workload requirements while remaining within the percent hardware utilization limits.

A3

2. (unchanged) A method as recited in claim 1, the method further comprising the steps of:

accepting user entered changes to the percent hardware utilization limits;

recalculating the required hardware resources in order to remain within

said percent hardware utilization limits; and

outputting the required hardware resources to the human

user in a format to advise the human user.

A3

3. (unchanged) A method as recited in claim 1, the method further comprising the steps of:

obtaining database requirements; and

calculating the hardware resources needed to satisfy the database requirements while remaining within the percent hardware utilization limits.

4. (canceled) A method as recited in claim 4, the method further comprising the steps of:

accepting user entered changes to the percent hardware utilization limits; recalculating the required hardware resources in order to remain within said percent hardware utilization limits; and

outputting the required hardware resources to the human user in a format to advise the human user.

SUB C2

5. (amended) A method as recited in claim 2, wherein the throughput workload requirement includes a transactions per second requirement.

A4

6. (unchanged) A method as recited in claim 5, wherein the calculating and recalculating steps include calculating the

hardware resources needed as a function of the transactions per second.

7. (unchanged) A method as recited in claim 4, wherein said hardware resource requirements include a number of processors.

8. (unchanged) A method as recited in claim 7, wherein said calculating and recalculating steps include calculating said number of processors as a function of the transactions per second.

9. (unchanged) A method as recited in claim 4, wherein the percent hardware utilization limits include percent processor utilization and said accepting step includes accepting changes to said processor utilization and said calculation and recalculation steps includes calculating said hardware requirements within said processor utilization limits and include changing said number of processors required when necessary to remain within said processor utilization limits.

10. (unchanged) A method as recited in claim 9, wherein said processor utilization limits include upper utilization limits to prevent over utilizing said processors and said

calculating and recalculating steps include calculating said number of processors needed keeping below said upper limit to prevent over utilization of said processors.

11. (unchanged) A method as recited in claim 10, wherein said processor utilization limits include lower utilization limits to prevent under utilizing said processors.

12. (unchanged) A method as recited in claim 11, wherein said calculating and recalculating steps include calculating said number of processors needed keeping above said lower limit to prevent under utilization of said processors.

13. (unchanged) A method as recited in claim 10, wherein said percent hardware utilization limits include percent network interface card utilization and said calculating and recalculating steps include calculating said hardware requirements within said network interface card utilization limits and include changing said number of network interface cards required when necessary to remain within said network interface card utilization limits.

14. (unchanged) A method as recited in claim 13, wherein said network interface card utilization limits include lower

utilization limits to prevent under utilizing said network interface cards and said calculating and recalculating steps include calculating said number of network interface cards needed keeping above said lower limit to prevent under utilization of said network interface cards.

15. (unchanged) A method as recited in claim 14, wherein said network interface card utilization limits include upper utilization limits to prevent over utilizing said network interface cards and said calculating and recalculating steps include calculating said number of network interface cards needed keeping below said upper limit to prevent over utilization of said network interface cards.

16. (unchanged) A computerized method for calculating hardware requirements for a database management system computer comprising the steps of:

establishing default values for hardware utilization limits;

initializing said hardware utilization limits to said default values;

obtaining a workload requirement from said human user; and

calculating said hardware requirements as a function of said workload requirement while remaining within said hardware

utilization limits.

17. (unchanged) A computerized method as recited in claim 16, the method further comprising the steps of:

obtaining new hardware utilization limits from said human user;

recalculating said hardware requirements while remaining within said hardware utilization limits; and

displaying hardware requirements in a format to advice the user of the required hardware for the user entered workload.

18. (unchanged) A computerized as recited in claim 17, wherein said hardware requirements include discrete numbers of hardware components.

19. (unchanged) A computerized method as recited in claim 18, wherein and said calculating and recalculating steps include calculating said number of hardware component.

DISCUSSION

In paragraph 1 of the Office Action, the Examiner said that the attempt to incorporate subject matter into this application by reference to "Co-Pending Applications" is improper because the U.S. Patent Application Numbers and filing dates have not

been supplied. In response, Applicant has amended pages 1, 12 and 13 of the specification to fill in the blanks and make a correction.

The examiner objected to claim 4 under 37 CFR 1.75 as being a substantial duplicate of claim 2. Also, claim 4 depended from itself. Claim 4 is canceled and claim 5 is amended to depend from claim 2.

Claim 1 was rejected by the examiner under 35 U.S.C. 103(a) as being unpatentable over Deluca et al. (U.S. Patent No. 5,848,270), Litzenberger (U.S. Patent No. 5,870,460), and Shannon et al. (U.S. Patent No. 6,088,678). The examiner indicated that Deluca et al. rendered obvious independent claim 1 by the following language: "...providing one or more percent...utilization limits..." at col. 12, lines 6-10; "...hardware..." at col. 5, lines 30-33; "...while remaining within the percent...utilization limits..." at col. 12, lines 6-10. Lines 30-33 of col. 5 state: "As mentioned above, the process of determining the appropriate size or hardware for each of systems 202, 204, and 206 is referred to as 'sizing' of the server system." This appears to be a definition of "sizing" in the context of DeLuca et al. The sentence of col. 12, lines 6-10, is: "However, because the present invention limits the actual utilization to less than 75 percent for each CPU, four of the existing CPUs each operating at a 75 percent utilization are

required to perform the workload." DeLuca et al. teach a limit of utilization away from claim 1 which refers to a minimum of utilization of "one or more percent." According to claim 1, utilization could be greater than 75 percent.

The examiner said that Litzenberger teaches the use of throughput workload requirements as follows: "...obtaining throughput...requirements..." at col. 2, lines 4-8; "...workload..." at col. 3, lines 27-29; and "...needed to satisfy the...requirements..." at col. 2, lines 4-8 The statement of lines 4-8 of col. 2 is: "As the long distance carriers constantly strive to provide more enhanced intelligent networking technologies and services, projections show that the throughput requirements will grow much faster than the processing capabilities of the network." The sentence in lines 27-29 of col. 3 is: "As stated above, the round-robin selection distributes workload across the data links 101, 103, 101", 103", 101Δ, and 103Δ evenly." Litzenberger relates to a system for the least cost routing of data transactions in a telecommunications network. The Applicant would not have considered this patent as analogous art. The examiner said that it would have been obvious to one ordinarily skilled in the art at the time of the invention to use throughput workload requirements in order to determine how much work the computer hardware would be required to perform to justify hardware

upgrades. The Applicant is not aware of the relevance of this statement relative to the Litzenberger cite.

The examiner stated that Shannon teaches the use of calculating the required resources in the words of "...calculating the...resources..." at col. 1, lines 66-67 and col. 2, lines 1-6. The statement from these lines is: "To meet the above and other objectives, the present invention provides for an improved computer-implemented process simulation method or tool that uses a software engine that calculates resources required to complete a project based upon contents of user-defined benefit-trade matrices associated with substeps of the project and design requirement priority values and a sample design whose process is to be simulated." Shannon pertains to a process simulation technique using benefit-trade matrices to estimate schedule, cost, and risk. Also, the examiner said that it would have been obvious to one ordinarily skilled in the art at the time of the invention to calculate the hardware resources required for a system in order to estimate the cost of hardware upgrades. The present application talks about hardware resources and Shannon refers resources, including people, tools and machines, for accomplishing a substep of designing and building a computer system. There appears to be a difference in meanings of the term "resources" in Shannon and the present application.

Claims 2 and 4 were rejected by the examiner under 35 U.S.C. 103(a) as being unpatentable over Deluca, Litzenberger, and Shannon as applied to claim 1 above, and further in view of Kayahara (U.S. Patent No. 6,405,206). Claim 4 has been cancelled by this amendment. However, as to claim 2, the examiner indicated that the "...to the percent...utilization limits...," is taught by Deluca at col. 12, lines 6-10; the "...hardware...," is taught by Deluca at col. 5, lines 30-33; the "...recalculating the required...resources...," is taught by Shannon at col. 1, lines 66- 67 and col. 2, lines 1-6; the "...hardware...," is taught by Deluca at col. 5, lines 30-33; the "...in order to remain within said percent...utilization limits...," is taught by Deluca at col. 12, lines 6-10; the "...hardware...," is taught by Deluca at col. 5, lines 30-33; the "...the required...resources...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6; and the "...hardware...," is taught by Deluca at col. 5, lines 30-33. The examiner seems to be saying that the words or terms themselves rather than the concepts or elements of the respective claims are taught by the prior art. Further, it appears that the examiner assumes that the meanings of the terms, whatever their context, are the same in the cited art and the present application.

The examiner said that Kayahara teaches the use of user input and the outputting of data in formats in the following quoted paragraphs.

> "An information search processing device in accordance with the invention comprises memory means that stores multiple types of searching strategies that show ways of information searching, user input controlling means that accepts a searching request of a user, reads out the multiple types of searching strategies from said memory means, and displays them on a display means to enable the user to select an arbitrary searching strategy among the multiple types of searching strategies, and searching means that performs information searching with respect to the searching request which was input by the user in accordance with the searching strategy which is selected by the user." (Col. 3, lines 25-37.)
>
> "Therefore, it is an object of the invention to dramatically decrease the burden of the searching operation which is performed by the user, make information searching possible by a searching method which the user desires, and make it possible to output a search result by categorizing and coordinating into a format the user desires." (Col. 1, lines 59-64.)

The examiner added that it would have been obvious to one ordinarily skilled in the art at the time of the invention to allow user input and to output the results of the calculations in a defined format in order to provide the user with the capability of changing the previously defined data and to provide the user feedback in a meaningful format. Kayahara discloses searching information from the Internet, for example, and the way for displaying searched information. The searching and editing are performed in accordance with the characteristic

of the editor selected by the user and the edited result is displayed. The issue there is getting the information that user desires.

Claims 3 and 5-15 are ultimately dependent from claim 1, and if claim 1 were to be allowed they would be also in virtue of their dependency. The rejections of claims 3 and 5-15 are summarized below.

Claim 3 was rejected by the examiner under 35 U.S.C. 103(a) as being unpatentable over DeLuca, Litzenberger, and Shannon as applied to claim 1 above, and further in view of Oulid-Aissa et al. (U.S. Patent No. 5,835,757). As to claim 3, the examiner indicated that the "...obtaining...requirements...," is taught by Shannon at col. 1, lines 13-18; the "...and calculating the...resources ...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6; the "...hardware...," is taught by Deluca at col. 5, lines 30-33; the "...while remaining within the percent...utilization limits...," is taught by Deluca at col. 12, lines 6-10; and the "...hardware...," is taught by Deluca at col. 5, lines 30-33.

The examiner stated that Oulid-Aissa teaches the use of database requirements as follows: "...New database requirements impacting data structures, contents, or access techniques may then be added without impact to the applications..." at col. 5, lines 52-54. The examiner further stated, "It would have been

obvious to one ordinarily skilled in the art at the time of the invention to use database requirements when defining a computer system in order to provide a means of storing data used by the application programs."

Claims 5-9 were rejected by the examiner under 35 U.S.C. 103(a) as being unpatentable over Deluca, Litzenberger, Shannon, and Kayahara as applied to claim 4 above, and further in view of Kulkarni et al. (U.S. Patent No. 6,138,016). As to claim 5, the examiner said that the "…throughput...requirement…,"is taught by Litzenberger at col. 2, lines 4-8; and the "...workload...," is taught by Litzenberger at col. 3, lines 27-29.

The examiner indicated that Kulkarni teaches the use of the transactions per second requirement in the following statement.

> "To overcome the requirement of localizing the HLR in a single expensive machine, with a very high rate of messages per second and data base transactions per second, and according to this invention, the HLR function is distributed across multiple processors." (Col. 1, lines 58-62.)

The examiner also said that it would have been obvious to one ordinarily skilled in the art at the time of the invention to use the measure transactions per second for workload throughput in order to use a widely used measure and gain acceptance for this method of sizing computer hardware requirements.

As to claim 6, the examiner stated that the "...calculating and recalculating steps include calculating the...resources

needed...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6; the "...hardware...," is taught by Deluca at col. 5, lines 30-33; and the ''...as a function of the transactions per second...," is taught by Kulkarni at col. 1, lines 58-62.

As to claim 7, the examiner said that the "...hardware...," is taught by Deluca at col. 5, lines 30- 33; the "...resource...," is taught by Litzenberger at col. 2, lines 14-18; and the "...include a number of processors...," is taught by Kulkarni at col. 2, lines 13-29.

As to claim 8, the examiner indicated that the "...calculating and recalculating steps include calculating...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6; the "...said number of processors...," is taught by Kulkarni at col. 2, lines 13-29; and the "...as a function of the transactions per second...," is taught by Kulkarni at col. 1, lines 58-62.

As to claim 9, the examiner stated that the "...percent...utilization limits include percent...utilization...," is taught by Deluca at col. 12, lines 6-10; the "...hardware...," is taught by Deluca at col. 5, lines 30-33; the "...processor...," is taught by Kulkarni at col. 2, lines 13-29, the "...and said accepting step includes accepting changes...," is taught by Kayahara at col. 3, lines 25-37; the "...to said...utilization...," is taught by Deluca at col. 12,

lines 6-10; the "...processor...," is taught by Kulkarni at col. 2, lines 13-29; the "...and said calculation and recalculation steps includes calculating...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6; the "...said hardware...,"is taught by Deluca at col. 5, lines 30-33; the "...requirements...," are taught by Litzenberger at col. 2, lines 4-8; the "...within said...utilization limits...," is taught by Deluca at col. 12, lines 6-10; the "...processor...," is taught by Kulkarni at col. 2, lines 13-29; the "...and include changing said number of processors required...," is taught by Kulkarni at col. 2, lines 13-29; the "...when necessary to remain within said...utilization limits...," is taught by Deluca at col. 12, lines 6-10; and the "...processor...," is taught by Kulkarni at col. 2, lines 13-29.

Claims 10-12 were rejected by the examiner under 35 U.S.C. 103(a) as being unpatentable over Deluca, Litzenberger, Shannon, Kayahara, and Kulkarni as applied to claim 9 above, and further in view of Itoh et al. (U.S. Patent No. 5,802,308) and Obhan (U.S. Patent No. 6,275,695). As to claim 10, the examiner said that "...processor...," is taught by Kulkarni at col. 2, lines 13-29; the "...utilization limits...," is taught by Deluca at col. 12, lines 6-10; the "...and said calculating and recalculating steps include calculating...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6; the

"...said number of processors needed...," is taught by Kulkarni at col. 2, lines 13-29; and the "...of said processors...," is taught by Kulkarni at col. 2, lines 13-29.

The examiner indicated that Itoh teaches the use of upper utilization limits and being under the upper limits in the following quotes.

> "The upper and lower limit values are respectively designated as X1 and X2 for the utilization of the central control unit, Y1 and Y2 for the utilization of the shared resources, and Z1 and Z2 for the response processing time." (Col. 4, lines 59-63.)
> "The effect of the control has now begun to show, and at time t4, the load or utilization drops below the upper limit but still above the lower limit, so that the level 3 is maintained." (Col. 6, lines 41-44.)

The examiner added that it would have been obvious to one ordinarily skilled in the art at the time of the invention to set upper utilization limits on a processor and to operate below those limits in order to avoid overload of the system, and possibly have system failure.

The examiner stated that Obhan teaches the over utilization of system resources in the following statement.

> "Each time the BTS resource reaches a BTS watermark a signal is sent to the SYM server 324 to apprise the SYM server 324 of such under or over utilization." (Col. 10, lines 54-57.)

The examiner said that it would have been obvious to one ordinarily skilled in the art at the time of the invention to

avoid overload of the system in order to prevent this cause of system failure.

As to claim 11, the examiner stated that the "...processor...," is taught by Kulkarni at col. 2, lines 13-29; the "...utilization limits...," is taught by Deluca at col. 12, lines 6-10; the "...include lower utilization limits...," is taught by Itoh at col. 4, lines 59-63; the "...to prevent under utilizing...," is taught by Obhan at col. 10, lines 54-57; and the "...said processors...," is taught by Kulkarni at col. 2, lines 13-29.

As to claim 12, the examiner said that the "...calculating and recalculating steps include calculating...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6; the "...said number of processors needed...," is taught by Kulkarni at col. 2, lines 13-29; the "...keeping above said lower limit...," is taught by Itoh at col. 6, lines 41-44; the "...to prevent under utilization...," is taught by Obhan at col. 10, lines 54-57; and the "...of said processors...," is taught by Kulkarni at col. 2, lines 13-29.

Claims 13-15 were rejected by the examiner under 35 U.S.C. 103(a) as being unpatentable over Deluca, Litzenberger, Shannon, Kayahara, Kulkarni, Itoh, and Obhan as applied to claim 9 above, and further in view of Fletcher et al. (U.S. Patent No. 6,108,782). As to claim 13, the examiner indicated the

"...percent...utilization limits include percent...utilization...," is taught by Deluca at col. 12, lines 6-10; the "...hardware...," is taught by Deluca at col. 5, lines 30-33; the "...and said calculating and recalculating steps include calculating...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6; the "...said hardware...," is taught by Deluca at col. 5, lines 30-33;, the "...requirements...," is taught by Litzenberger at col. 2, lines 4-8; the "...utilization limits...," is taught by Deluca at col. 12, lines 6-10; and the "...required when necessary to remain within...utilization limits...," is taught by Deluca at col. 12, lines 6-10.

The examiner stated that Fletcher teaches the use of network interface cards as follows:

> "According to the present invention, collectors and agents may be designed to operate effectively with a number of different network interface cards (NICs) and NOS architectures and a number of different management applications." (Col. 15, lines 61-64.)

The examiner added that it would have been obvious to one ordinarily skilled in the art at the time of the invention to use network interface cards in order to communicate between processors in the system.

As to claim 14, the examiner indicated that the "...network interface card...," is taught by Fletcher at col. 15, lines 61-

64; the "...utilization limits...," is taught by Deluca at col. 12, lines 6-10; the "...include lower utilization limits...," is taught by Itoh at col. 4, lines 59-63; the "...to prevent under utilizing...," is taught by Obhan at col. 10, lines 54-57; the "...said network interface cards...," is taught by Fletcher at col. 15, lines 61-64; the "...and said calculating and recalculating steps include calculating...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6; the "...said number of network interface cards...," is taught by Fletcher at col. 15, lines 61- 64; the "...needed keeping above said lower limit...," is taught by Itoh at col. 6, lines 41-44; the "...to prevent under utilization...," is taught by Obhan at col. 10, lines 54-57; and the "...of said network interface cards ," is taught by Fletcher at col. 15, lines 61-64.

As to claim 15, the examiner stated that the "...network interface card...," is taught by Fletcher at col. 15, lines 61-64; the "...utilization limits...," is taught by Deluca at col. 12, lines 6-10; the "...include upper utilization limits...," is taught by Itoh at col. 4, lines 59-63; the "...to prevent over utilizing...," is taught by Obhan at col. 10, lines 54-57; the "...said network interface cards...," is taught by Fletcher at col. 15, lines 61-64; the "...and said calculating and recalculating steps include calculating...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6; the

"...said number of network interface cards needed...," is taught by Fletcher at col. 15, lines 61-64; the "...keeping below said upper limit...," is taught by Itoh at col. 6, lines 41-44; the "...to prevent over utilization...," is taught by Obhan at col. 10, lines 54-57; and the "...of said network interface cards...," is taught by Fletcher at col. 15, lines 61- 64.

Independent claim 16 was rejected by the examiner under 35 U.S.C. 103(a) as being unpatentable over Coss et al. (U.S. Patent No. 5,538,423), Deluca, Shannon, Litzenberger, and Kulkarni. The examiner said that Coss rendered obvious independent claim 16 by the following: "...establishing default values..." at col. 19, lines 54-57. "...for hardware..." at col. 19, lines 40-41; "...initializing said hardware..." at col. 19, lines 40-41; "...to said default values..." at col. 19, lines 54-57; "...hardware..." at col. 19, lines 40-41; and "...hardware..." at col. 19, lines 40-41.

Coss et al. pertain to an apparatus for controlling operational parameters of a surgical drilling system. The applicant believes that this art is non-analogous.

The examiner indicated that Deluca teaches the use of utilization limits as follows: "...utilization limits..." at col. 12, lines 6-10; "...utilization limits..." at col. 12, lines 6-10; and "...while remaining within said...utilization limits..." at col. 12, lines 6-10. The examiner added that it

would have been obvious to one ordinarily skilled in the art at the time of the invention to use hardware utilization limits in order to define the extent that hardware may be used without risking failure.

The examiner stated that Shannon teaches obtaining requirements from users and calculating requirements as follows: "...obtaining a...requirement from said human user..." at col. 1, lines 14-19; "...calculating said...requirements..." at col. 2, lines 27-33; and "...requirement..." at col. 1, lines 14-19. The examiner also stated that it would have been obvious to one ordinarily skilled in the art at the time of the invention to allow user input in order to provide the user with the capability of changing the previously defined data. The examiner added that, likewise, it would have been obvious to one ordinarily skilled in the art at the time of the invention to calculate the hardware resources required for a system in order to estimate the cost of hardware upgrades.

The examiner said that Litzenberger teaches the use of workloads as follows: "...workload..." at col. 3, lines 27-29; and "...of said workload..." at col. 3, lines 27-29. The examiner further said that it would have been obvious to one ordinarily skilled in the art at the time of the invention to use workload requirements in order to determine how much work

the computer hardware would be required to perform to justify hardware upgrades.

The examiner indicated that Kulkarni teaches the use of functions as follows, "...as a function..." at col. 1, lines 58-62. The examiner said that it would have been obvious to one ordinarily skilled in the art at the time of the invention to use functions in order to establish relationships between component hardware parameters of a system and the performance of the system.

The applicant does not see the suggestion or motivation above for the combination of Coss et al., Deluca et al., Shannon, Litzenberger and Kulkarni et al., used to reject claim 16.

Claims 17-19 are ultimately dependent from claim 16, and if claim 16 were to be allowed they would be also in virtue of their dependency. The rejections of claims 17-19 are summarized below.

Claim 17 was rejected by the examiner under 35 U.S.C. 103(a) as being unpatentable over Coss, Deluca, Shannon, Litzenberger, and Kulkarni as applied to claim 16 above, and further in view of Kayahara. As to claim 17, the examiner said that the "...obtaining new...utilization limits...," is taught by Deluca at col. 12, lines 6-10; the "...hardware...," is taught by Deluca at col. 5, lines 30-33; the "...from said human

user...," is taught by Shannon at col. 1, lines 14-19; the "...recalculating said ...requirements...,' is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-6; the "...hardware...," is taught by Deluca at col. 5, lines 30-33; the "...while remaining within said...utilization limits...," is taught by Deluca at col. 12, lines 6-10; the "...hardware...," is taught by Deluca at col. 5, lines 30-33; the "...hardware requirements...," is taught by Deluca at col. 6, lines 11-14; the "...of the required hardware...," is taught by Deluca at col. 6, lines 11-14; the "...for the user entered...," is taught by Shannon at col. 1, lines 14-19; and the "...workload...," is taught by Litzenberger at col. 3, lines 27-29.

The examiner indicated that Kayahara teaches the outputting of data in formats in the following paragraph.

> "Therefore, it is an object of the invention to dramatically decrease the burden of the searching operation which is performed by the user, make information searching possible by a searching method which the user desires, and make it possible to output a search result by categorizing and coordinating into a format the user desires" (Col. 1, lines 59-64.)

The examiner added that it would have been obvious to one ordinarily skilled in the art at the time of the invention to output the results of the calculations in a defined format in order to provide the user feedback in a meaningful format.

Claims 18 and 19 were rejected by the examiner under 35 U.S.C. 1.03(a) as being unpatentable over Coss, Deluca, Shannon, Litzenberger, Kulkarni, and Kayahara as applied to claim 17 above, and further in view of Leatham et al. (U.S. Patent No. 6,370,383). As to claim 18, the examiner stated that the "...hardware requirements...," is taught by Deluca at col. 6, lines 11-14.

The examiner said that Leatham teaches the use of discrete numbers of hardware components in the following statements.

> "Here, however, as each sectors 40-1 through 40-3 has a discrete number of radio transceivers serving that sectors, it is contemplated that, based on changes in the operation of the radio transceivers in each one of the sectors 40-1, 40-2 and 40- 3, the MPT 46-1, 46-2 and 46-3 could be dramatically different for each respective sector 40-1, 40-2 and 40-3 of the sectored cell 40'." (Col. 15, lines 43-50.)
>
> "Thus, the base station 14, the ICP 15 and the MSC 18 include a number of hardware and/or software components that are not described and illustrated herein." (Col. 7, lines 44-46.)

The examiner stated, "It would have been obvious to one ordinarily skilled in the art at the time of the invention to use a discrete number of hardware components in order to have individually distinct hardware components and provide a more robust method of sizing a computer system."

As to claim 19, the examiner indicated that the "...calculating and recalculating steps include calculating...," is taught by Shannon at col. 1, lines 66-67 and col. 2, lines 1-

6; and the "...said number of hardware components...," is taught by Leatham at col. 7, lines 44-46.

The Applicant respectfully disagrees with the rejections or in some instances with the bases of the rejections. To recap; in essence, this office action appears to reveal a different style of examination that the Applicant has not previously encountered. The rejection of many elements of the claims appears to have been done with seemingly isolated references, and in some instances the rejection of various portions of the same element was effected by different references or by different unconnected parts of the same reference. In some places of a rejection, a single term or word in an element was rejected with an isolated portion of a reference. Some of the cited portions or terms of the reference appeared to be taken out of context. Many of the references did not all appear to be from the same field of art of the present invention or even relative to each other. The suggestion or the motivation for combining elements or terms from the several or many various cited references might be regarded as being readily apparent to the Applicant. In this light, one could go to a technical encyclopedia, dictionary, patent database or the net and search for the terms or elements of claims for rejection purposes.

Often, a statement of obviousness of a combination relative to a rejected element or term of a claim appeared to be

conclusory in that the specific suggestion or motivation for the combination was not clearly pointed out or stated. Further, there appeared to be no evident suggestion in the cited art or motivation for the combining many of the referred-to parts of the numerous references cited to reject a claim, or for the total combination of "old" elements or terms from the references being asserted in the rejection of the respective claim. It appears then that any claim with elements or portions of elements findable in some prior art would not be allowable. It seems to follow that it would be futile to amend a rejected claim if a newly added limitation or portions of it were somehow existent anywhere in the prior art.

The following information and cases are cited here to support the Applicant's position even though the Examiner may be well aware of them. Because an element can be found somewhere in a prior art, analogous or not, does not mean that the claim is unallowable. "As this court [the Federal Circuit] has stated, 'virtually all [inventions] are combinations of old elements.' Environmental Designs, Ltd. v. Union Oil Co., 713 F.2d 693, 698, 218 USPQ 865, 870 (Fed. Cir. 1983); see also Richdel, Inc. v. Sunspool Corp., 714 F.2d 1573, 1579-80, 219 USPQ 8, 12 (Fed. Cir. 1983) ("Most, if not all, inventions are combinations and mostly of old elements."). Therefore an examiner may often find every element of a claimed invention in

the prior art. If identification of each claimed element in the prior art were sufficient to negate patentability, very few patents would ever issue. Furthermore, rejecting patents solely by finding prior art corollaries for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention. Such an approach would be "an illogical and inappropriate process by which to determine patentability.' Sensonics, Inc. v. Aerosonic Corp., 81 F.3d 1566, 1570, 38 USPQ2d 1551, 1554 (Fed. Cir. 1996)." In re Rouffet, 47 USPQ 1453, 1457 (Fed. Cir. 1998).

The following case, though not necessarily binding precedent, seems to suggest that if a claim is not allowable, that a rejection preferably be based on fewer references. "The examiner concluded that applicant's invention would have been obvious in light of twelve references. The Board correctly stated that the examiner's reliance on so many references was "overkill" and concluded that applicant's invention would have been obvious in light of four of the references. We agree with the Board on the former statement, but disagree with the latter. What both the examiner and Board have done is to cite a number of references variously containing some of the limitations in applicant's claims. However, these references and the limitations for which they were cited were combined piecemeal

without any suggestion or motivation for their combination and without regard to the purpose of applicant's invention. . . ." In re Blamer, Civ. App. No. 93-1108, slip op. at 3-4 (Fed. Cir. Sept. 21, 1993) (unpublished).

"When relying on numerous references or a modification of prior art, it is incumbent upon the examiner to identify some suggestion to combine references or make the modification." In re Jones, 958 F.2d 347, 351, 21 USPQ2d 1941, 1943 (Fed. Cir. 1992) (stating that there must be some suggestion to combine, "either in the references themselves or in the knowledge generally available to one of ordinary skill in the art"); see Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 292, 227 USPQ 657, 664 (Fed. Cir. 1985)." In re Mayne, 41 USPQ2d 1451, 1454 (Fed Cir. 1997).

"'The factual inquiry whether to combine references must be thorough and searching.' Id. [McGinley v. Franklin Sports, Inc., 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001)] It must be based on objective evidence of record. This precedent has been reinforced in myriad decisions, and cannot be dispensed with. See, e.g., Brown & Williamson Tobacco Corp. v. Philip Morris Inc., 229 F.3d 1120, 1124-25, 56 USPQ2d 1456, 1459 (Fed. Cir. 2000) ("a showing of a suggestion, teaching, or motivation to combine the prior art references is an 'essential component of an obviousness holding'") (quoting C.R. Bard, Inc.,

v. M3 Systems, Inc., 157 F.3d 1340, 1352, 48 USPQ2d 1225, 1232 (Fed. Cir. 1998)); In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999) ("Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references."); In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998) (there must be some motivation, suggestion, or teaching of the desirability of making the specific combination that was made by the applicant); In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) ("'teachings of references can be combined only if there is some suggestion or incentive to do so.'") (Emphasis in original) (quoting ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984))." In re Lee, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).

The suggestion or motivation for combining various references should be specific. "The need for specificity pervades this authority. See, e.g., In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) ("particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed"); In re Rouffet, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir.

1998) ("even when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combination. In other words, the Board must explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious."); In re Fritch, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (the examiner can satisfy the burden of showing obviousness of the combination "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references")." In re Lee, 61 USPQ2d 1430, 1433-34 (Fed. Cir. 2002).

"Our case law makes clear that the best defense against hindsight-based obviousness analysis is the rigorous application of the requirement for a showing of a teaching or motivation to combine the prior art references. See In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). 'Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability--the essence of hindsight.' Id." Ecolochem Inc. v. Southern California Edison Co., 56 USPQ2d 1065, 1073 (Fed. Cir. 2000). As noted in In re Fritch, 23 USPQ 2d 1780, 1784

(Fed. Cir. 1992), it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. The court has stated that "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." (quoting In re Fine, 837 F.2d 1071, 1075, 5 USPQ 2d 1596, 1600 (Fed. Cir. 1988). To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher. W.L. Gore & Associates, Inc. v. Garlock, Inc., 220 USPQ 303, 312-13 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

The cited reference should be analogous prior art. "To ascertain the scope of the prior art, a court examines 'the field of the inventor's endeavor,' Shatterproof Glass Corp. v. Libbey-Owens Ford Co., 758 F.2d 613, 620, 225 USPQ 634, 638 (Fed. Cir. 1985), and 'the particular problem with which the inventor was involved,' Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 1535, 218 USPQ 871, 876 (Fed. Cir. 1983) (quoting In re Wood, 599 F.2d 1032, 1036, 202 USPQ 171, 174 (CCPA 1979)), at the 'time the invention was made,' see 35 U.S.C. § 103(a)."

Monarch Knitting Machinery Corp. v. Sulzer Morat GmbH, 45 USPQ2d 1977, 1981 (Fed. Cir. 1998).

An instance of art appearing to be analogous, e.g., memories, but not so, was discussed by the Federal Circuit in the following. "The Allen-Bradley art is not in the same field of endeavor as the claimed subject matter merely because it relates to memories. It involves memory circuits in which modules of varying sizes may be added or replaced; in contrast, the subject patents teach compact modular memories." Wang Laboratories, Inc. v. Toshiba Corp., 26 USPQ 2d 1767, 1773 (Fed. Cir. 1993). Further, "Wang's SIMMs were designed to provide compact computer memory with minimum size, low cost, easy repairability, and easy expandability. . . . In contrast, the Allen-Bradley patent relates to a memory circuit for a larger, more costly industrial controller. . . . Thus, there is substantial evidence in the record to support a finding that the Allen-Bradley prior art is not reasonably pertinent and is not analogous." Id.

Some of the statements regarding obviousness of a certain element or elements of a claim in view of cited references appeared to be conclusory. "'Broad conclusory statements regarding the teaching of multiple references, standing alone, are not "evidence."' Dembiczak, 175 F.3d at 999, 50 USPQ2d at

1617." Ecolochem Inc. v. Southern California Edison Co., 56 USPQ2d 1065, 1073 (Fed. Cir. 2000).

The Applicant respectfully requests that the claim examination process used by the Examiner in the present office action be reconsidered in view of the concerns stated above by the Applicant. The Applicant also respectfully requests reconsideration of the pending claims, and allowance of these claims.

Respectfully submitted,

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By their Attorney,

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